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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,840	12/11/2003	Alex Chughen Chow	AUS920030713US1	2185

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EXAMINER	
TRUONG, CAMQUY	
ART UNIT	**PAPER NUMBER**
2195	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,840	CHOW, ALEX CHUGHEN	
	Examiner	Art Unit	
	Camquy Truong	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1- 22 are presented for examination.

2. It is noted that although the present application does contain line numbers in the specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the examiner and Applicant all future correspondence should include the recommended line numbering.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7-8, 9-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following terms lack proper antecedent basis:

i. The kernel – claim 9, line 4.

B. The claim language in the following claims is not clearly understood:

i. As to claim 7, lines 4-9, it is uncertain how the step of " preloading ..." relates to step of " passing control...".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1,3 –7, 9-10, 12-15, 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundaresan (U.S. Patent 6,289,369 B1) in view of Willen et al. (U.S. Patent 7,159,221 B1).

7. As to claim 1, Sundaresan teaches the invention substantially as claimed including: a method for load balancing in a tightly-coupled multiprocessor computer system comprising the steps of:

placing a plurality of tasks into a centralized task queue (Fig. 2; threads 22 resident in the central schedule queue 26, col. 5, lines 62-63); and

distributing the plurality of tasks in the centralized task queue to a plurality of library processors (threads 22 can migrate among processor 10, col. 5, lines 62-64; col. 8, lines 24-27).

8. Sundaresan does not explicitly teach at least one task from the plurality of tasks in the centralized task queue is distributed to at least one of the plurality of library processors when the library processor has at least one empty task buffer. However,

Willen teaches at least one task from the plurality of tasks in the centralized task queue is distributed to at least one of the plurality of library processors when the library processor has at least one empty task buffer (the processor in the group become idle when the processor queue is empty, it may choose to steal work from the queue of another processor, col. 2, lines 54-56; col. 16, lines 28-39; col. 19, lines 50-65; col. 23, lines 1-7).

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of at least one task from the plurality of tasks in the centralized task queue is distributed to at least one of the plurality of library processors when the library processor has at least one empty task buffer as taught by Willen to the invention of Sundaresan because this allows to balance the system load while minimizing the overhead of fetching cached data from remote cache memories (col. 3, lines 12-14).

10. As to claim 3, Willen teaches distributing the task from the plurality of tasks in the centralized task queue to the one of a plurality of library processors when the one of a plurality of library processors has all of its task buffers empty; that is, when load of the one of a plurality of library processors is zero tasks (col. 2, lines 54-56; col. 16, lines 28-39; col. 19, lines 50-65; col. 23, lines 1-7).

11. As to claim 4, Willen teaches distributing the task from the plurality of tasks in the

centralized task queue to the one of the plurality of library processors by the one of a plurality of library processors fetching it from the centralized task queue (threads 22 can migrate among processor 10, col. 5, lines 62-64; col. 8, lines 24-27; col. 23, lines 1-7).

12. As to claims 5-6, Willen teaches distributing the task from the plurality of tasks in the centralized task queue to the one of the plurality of library processors by the one of the plurality of library processors fetching it from the centralized task queue when the load of the one of a plurality of library processors is zero or one tasks (col. 2, lines 54-56; col. 16, lines 28-39; col. 19, lines 50-65; col. 23, lines 1-7).

13. As to claim 7, Willen teaches method for avoiding latency in the distribution of a task from a centralized task queue to a library processor with a plurality of buffers, comprising the steps of:

preloading the task from the centralized task queue to an empty buffer of the plurality of buffers of the library processor (the processor in the group become idle when the processor queue is empty, it may choose to steal work from the queue of another processor, col. 2, lines 54-56; col. 16, lines 28-39; col. 19, lines 50-65; col. 23, lines 1-7); and

passing control to another task, ready for execution, contained in another buffer of the plurality of buffers of the library processor (the processor looks for the highest priority task on its own switching queue 122, and executes that task. If there is no task on the queue, then the processor is in idle state 124, then processor looks for another

processor that is significantly busier and that has a queue of tasks ready for execution. It will steal the highest priority task and execute, col. 22, line 65 – col. 23, line 8).

14. As to claim 9, it is rejected for the same reason as claim 1. In addition, Willen teaches a system kernel (Fig. 2; col. 5, lines 54-55).

15. As to claim 10, Willen teaches at least one of the plurality of library processors further comprises a library processor kernel and one or more task buffers, and wherein the system is further configured for a task placed in the library task queue to be distributed to one of the plurality of library processors when the library processor has at least one empty task buffer (col. 2, lines 54-56; col. 16, lines 28-39; col. 19, lines 50-65; col. 23, lines 1-7).

16. As to claims 12-13, Willen teaches the system kernel is comprised of a single processor (Fig. 2; col. 5, lines 49-53).

17. As to claim 14, it is rejected for the same reason as claim 4.

18. As to claim 15, it is rejected for the same reason as claim 1.

19. As to claim 17, it is rejected for the same reason as claim 5.

20. As to claims 18-20, it is rejected for the same reason as claim 4.

21. As to claim 21, it is rejected for the same reason as claim 7.

22. Claims 2, 8, 11, 16, 22, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundaresan (U.S. Patent 6,289,369 B1) in view of Willen et al. (U.S. Patent 7,159,221 B1), as applied to claims 1, 7, 9, 15, and 21 above, and further in view of Baumberger (U.S. Patent Application Publication 2005/0102671 A1).

23. As to claims 2, 8, 11, 16, 22, distributing the task from the plurality of tasks in the centralized task queue to the one of the plurality of library processors when the one of the plurality of library processors has one or two empty task buffers (col. 2, lines 54-56; col. 16, lines 28-39; col. 19, lines 50-65; col. 23, lines 1-7).
Sundaresan and Willen do not explicitly teach the one of the plurality of library processors has exactly two task buffers. However, Baumberger teaches teach the one of the plurality of library processors has exactly two task buffers (paragraph 16, lines 1-6).

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the one of the plurality of library processor has exactly two task buffers as taught by Baumberger to the invention of

Sundaresan and Willen because this allows computer program product for highly efficient, variable length data share between virtual machines.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Camquy Truong whose telephone number is (571) 272-3773. The examiner can normally be reached on 8AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3756.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Camquy Truong

September 22, 2006